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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,064	02/03/2004	Romel N. Manatad	018865-012810US	4533

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EXAMINER	
BREWSTER, WILLIAM M	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/772,064	MANATAD, ROMEL N.	
	Examiner	Art Unit	
	William M. Brewster	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 21-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 21-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 4-6, 23, 24, 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Tsuda et al., US Publication No. 2002/0047501 A1.

Tsuda anticipates limitations from claim 1, a method for making a semiconductor package comprising: in fig. 1,

(a) molding a molding material 3 around a leadframe structure, not shown, having a die 1 attach region of a plurality of leads 10, p. 4, ¶ 75-81, wherein the die attach region is exposed through a window in the molding material, beneath 6; and

(b) after (a), mounting a semiconductor die to the die attach region using a flip chip mounting process, p. 8, ¶ 157;

limitations from claim 5, the method of claim 1, in fig. 1, wherein the die attach region comprising at least one aperture, below 6;

limitations from claim 6, the method of claim 1 wherein molding comprises placing the leadframe structure in a molding tool, p. 4, ¶ 91;

limitations from claim 23, the method of claim 1, in fig. 1 wherein a bottom surface of the die is substantially coplanar with a surface of the molding material, lower inner surface of 3;

limitations from claim 24, the method of claim 1, in fig. 1, wherein the leads have surfaces that are substantially coplanar with an exterior surface of the molding material, bottom of 3, wherein "substantially coplanar" is subjective to the viewer;

limitations from claim 26, the method of claim 1, in fig. 1, wherein after mounting, the die package is formed, and wherein an exposed backside of the die forms an electrical terminal, terminals attached to 4;

limitations from claim 4, the method of claim 1 further comprising, after (b): reflowing solder that is been the die attach region of the leadframe and the semiconductor die. While Tsuda does not specify the reflow, it is part of the flip chip method. Proffered as evidence is Ukita et al., US Publication No. 2003/0059979 A, specifying the reflow of (solder) bumps between the die and the leadframe, p. 1, ¶ 9.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuda as applied to claims 1, 4-6, 23, 24, 26 above, and further in view of Kasem et al., US Patent No. 6,392,290 B1.

Tsuda does not specify a plurality of leads including a source and gate lead, but Kasem does. Kasem teaches:

limitations from claim 7, in figs. 3A - 3B, the method of claim 1 further comprising depositing solder on the die attach region of the leadframe structure within the window, col. 4, line 10 - col. 5, line 9;

limitations from claim 8, the method of claim 1, col. 4, line 10 - col. 5, line 9; wherein the plurality of leads comprise a source lead 16 and a gate lead, 20, col. 4, line 10 - col. 5, line 9;

limitations from claim 9, in figs. 5A-5B, the method of claim 1 further comprising: attaching a heat plate structure to the leadframe structure, col. 10, lines 39-44.

Kasem gives motivation in col. 1, lines 36 - 57. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Kasem's process with Tsuda's invention would have been beneficial because it is a less expensive and simpler way to form a vertical power MOSFET.

Claims 2, 3, 21, 22, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuda in view of Kasem et al., US Patent No. 6,392,290 B1.

Tsuda teaches limitations from claim 1, a method for making a semiconductor package comprising: in fig. 1,

(a) molding a molding material 3 around a leadframe structure, not shown, having a die 1 attach region of a plurality of leads 10, p. 4, ¶ 75-81, wherein the die attach region is exposed through a window in the molding material, beneath 6; and

(b) after (a), mounting a semiconductor die to the die attach region using a flip chip mounting process, p. 8, ¶ 157;

limitations from claim 21, in fig. 1, the method of claim 2 wherein the die attached region comprises at least one aperture, below 6.

limitations from claim 22, in fig. 1, the method of claim 3 wherein the die attached region comprises at least one aperture, below 6.

Tsuda does not specify a vertical power MOSFET with source and gate leads, but Kasem does.

Kasem teaches limitations from claim 2, in fig. 1, wherein the semiconductor die comprises a vertical power MOSFET, col. 4, lines 10-35, for a flip-chip configuration, col. 10, lines 40-44;

limitations from claim 3, figs. 3A - 3B, wherein the plurality of leads include at least one source lead 16 and at least one gate lead 20, col. 4, line 10 - col. 5, line 9;

limitations from claim 25, the method of claim 1, in fig. 3A, further comprising depositing a first solder 16 on the die attach region, wherein the solder 15 will be deposited on the die attach region when the die is set on the die attach region, and depositing a second solder 16 the die.

Kasem gives motivation in col. 1, lines 36 - 57. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Kasem's process with Tsuda's invention would have been beneficial because it is a less expensive and simpler way to form a vertical power MOSFET.

Response to Arguments

Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection. Examiner notes there is no assignee on file at the USPTO for this application.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 571-272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

William M. Brewster

WILLIAM M. BREWSTER
PRIMARY EXAMINER

10 April 2006
WB